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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,367	12/28/2001	Seiichi Iwasa	1466.1052	3361

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EXAMINER	
WARD, AARON S	

ART UNIT	PAPER NUMBER
2675	4

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,367	IWASA ET AL.	
	Examiner	Art Unit	
	Aaron S. Ward	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 10-18* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities. Although the Specification was checked for informalities, Applicant's cooperation is appreciated in correcting any additional informalities. For example, page 29, lines 14-18 and 26-28, discloses "cramp" elements. Should the Specification disclose "clamp" elements, as known in the art?

Appropriate correction is required.

Claim Objections

2. Claims 7 and 16 are objected to because of the following informalities: the claims recite "cramp circuit," but is "clamp circuit" intended as is known in the art? Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-8, 10-12 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kishi et al. (U.S. Patent No. 6,686,912).

As to claim 1, Kishi et al. teaches a method for driving a plasma display ay applying increasing cell voltage during reset (Fig. 45), including supplying increasing voltage to an

impedance conversion circuit 31' (Fig. 44) with output impedance lower than input, and supplying impedance conversion circuit output to the cells 20.

As to claim 2, Kishi et al. teaches a display driving device including a waveform generation circuit including capacitance element C4 (Fig. 44) and a constant-current source SW9' supplying current to capacitance element C4 when a control signal is active to generate an increasing voltage waveform, an impedance conversion circuit 31' for reducing output impedance of the waveform generation circuit SW9', C4, and a switch circuit SW5', Tr23 for connecting an input terminal to output terminal of impedance conversion circuit 31' when the control signal is not active.

As to claim 4, Kishi et al. teaches that the impedance conversion circuit includes MOSFETs in Fig. 44, and that a voltage control type transistor (col. 19, lines 12-14; Fig. 13B) can be used in place of a MOSFET e.g., in the impedance conversion circuit.

As to claim 5, Kishi et al. teaches that a diode (see SW9', Fig. 44) for preventing backflow is displosed between the capacitance element C4 and the constant-current source (see SW9').

As to claim 6, Kishi et al. teaches that a resistor R1 (see SW9', Fig. 44) is disposed between the capacitance element C4 and the constant-current source (see SW9').

As to claim 7, as best understood in view of the claim objections noted above regarding "cramp," Kishi et al. teaches the control signal is supplied to the constant current source via a clamp circuit SW4' for converting the control signal to a signal with respect to a power source potential Vs/2 as a reference of displacement (col. 44, lines 33-36).

As to claim 8, Kishi et al. teaches that the constant-current source SW9' (Fig. 44) includes a MOSFET, and that a voltage control type transistor including a variable resistor (Fig. 13B) can be used in place of a MOSFET for determining an output current value.

As to claim 10, Kishi et al. teaches a pair of waveform generation circuits (SW9' and C4, SW1' and C4), a pair of impedance conversion circuits (31' showing a pair of circuits) and a pair of switch circuits (SW5' and Tr23, SW4' and Tr22) wherein each of the pair circuits constitutes a complimentary symmetric circuit including semiconductor elements having different polarities for applying to plasma display panel 20 first/second increasing voltages having positive/negative gradients (Fig. 45 Y Electrode reset period).

As to claim 11, Kishi et al. teaches a display driving device including a waveform generation circuit including capacitance element C4 (Fig. 44) and a constant-current source SW9' supplying current to capacitance element C4 when a control signal is active to generate an increasing voltage waveform, an impedance conversion circuit 31' for reducing output impedance of the waveform generation circuit SW9', C4, and a switch circuit SW5', Tr23 for disconnecting an output OUTB' of waveform generation circuit SW9', C4 from an input of impedance conversion circuit 31' when the control signal is not active.

As to claim 12, Kishi et al. teaches that the impedance conversion circuit 31' includes a resistor R2 (Fig. 44) for connecting input and output of the impedance conversion circuit 31'.

As to claim 14, Kishi et al. teaches that the impedance conversion circuit includes MOSFETs in Fig. 44, and that a voltage control type transistor (col. 19, lines 12-14; Fig. 13B) can be used in place of a MOSFET e.g., in the impedance conversion circuit.

As to claim 15, Kishi et al. teaches that diode D17 for preventing backflow is disposed between the switch circuit SW5' and the impedance conversion circuit input.

As to claim 16, as best understood in view of the claim objections noted above regarding "cramp," Kishi et al. teaches the control signal is supplied to the constant current source via a clamp circuit SW4' for converting the control signal to a signal with respect to a power source potential Vs/2 as a reference of displacement (col. 44, lines 33-36).

As to claim 17, Kishi et al. teaches that the constant-current source SW9' (Fig. 44) includes a MOSFET, and that a voltage control type transistor including a variable resistor (Fig. 13B) can be used in place of a MOSFET for determining an output current value.

As to claim 18, Kishi et al. teaches a pair of waveform generation circuits (SW9' and C4, SW1' and C4), a pair of impedance conversion circuits (31' showing a pair of circuits) and a pair of switch circuits (SW5' and Tr23, SW4' and Tr22) wherein each of the pair circuits constitutes a complimentary symmetric circuit including semiconductor elements having different polarities for applying to plasma display panel 20 first/second increasing voltages having positive/negative gradients (Fig. 45 Y Electrode reset period).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishi et al. as applied to claims 2 and 11, respectively above, and further in view of Auger (U.S. Patent No. 3,754,230).

Kishi et al. teaches the invention as claimed in claims 2 and 11. Kishi et al. teaches that the impedance conversion circuit includes MOSFETs in Fig. 44, and that a plurality of transistors (col. 19, lines 12-14; Fig. 13B) can be used in place of a MOSFET e.g., in the impedance conversion circuit.

Kishi et al. does not specifically teach that the impedance conversion circuit includes a plurality of transistors in Darlington connection as recited in claims 3 and 13.

Auger teaches a plasma display system including output level control and output drive with two complimentary Darlington pair current amplifiers for driving a low impedance output from a high impedance input (col. 9, line 66 – col. 10, line 12; Fig. 14).

It would be obvious to combine the teaching of Auger with that of Kishi et al. because both references are directed to driving plasma displays supplying an output impedance lower than an input impedance. One would be motivated to make such a combination to obtain in Kishi et al. the benefit of driving a low impedance output from a high impedance input as taught by Auger, in view of the impedance conversion in Kishi et al.

Allowable Subject Matter

7. Claim 9 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aaron S. Ward whose telephone number is (703) 305-8992. The examiner can normally be reached on Monday - Friday, 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on (703) 305-9720. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASW

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